Filing Date: March 15, 2001

Title: DEVICE AND METHOD TO REDUCE WORDLINE RC TIME CONSTANT IN SEMICONDUCTOR MEMORY DEVICES

IN THE SPECIFICATION

On page 8, please amend the paragraph beginning on line 17 as follows. The changes support the amendment made to Figure 6 as discussed above. Applicant respectfully submits that no new matter is added with this amendment.

In this embodiment, the first wordline portion 313 is equal to the first half of the wordline, and the second wordline portion 314 is equal to the second half of the wordline. The strapping layers in this embodiment start at alternating ends of the memory array 200 and end in the middle of the memory array 200. This configuration reduces the RC time constant without increasing the size of the memory array 200. It should be noted, however, that in alternate embodiments the bypassed portions of wordlines could be shorter or longer than half of the wordline length, and the strapping layers may bypass middle portions 351 of the wordline instead of beginning or ending at the far ends of the wordlines. While only one strapping layer is used on each wordline in this embodiment, it should also be noted that multiple strapping layers could be used to bypass multiple portions 352 of each wordline. Multiple channels could also be used with one strapping layer to connect the strapping layer to the wordline.